Simulation Studies and Experiences of the preliminary CIGRE DC Grid Test System with EMTP-RV, PSCAD and Opal-RT

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Acknowledgement

- The work presented here was carried out by three different PhD students:
  - Wei Li (PSCAD)
  - Tetiana Bogodorova (EMTP-RV)
  - Rujiroj Leelaruji (Opal-RT Model: Matlab/Simulink/SPS + Lib.)
  - They worked very hard for several weeks! ☺
- We would like to thank the following persons for their support in using the models:
  - Luc-Andre Gregoire (Opal-RT)
  - Sebastien Dennetiere (RTE)
  - Juan Carlos Garcia Alonso (Manitoba HVDC Research Center)

To start

- **Be nice… ☺:** ***"No one loves the messenger who brings bad news"***
- About the test systems:
  - The specifications used in this work have been proposed by B4-57.
  - The specifications used to define the test system are preliminary and will be reviewed by the B4 WGs.

To start

- **Be nice… ☺: *"No one loves the messenger who brings bad news"***
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- Exercise judgment
  - Comparisons of highly detailed and complex models in three completely different software environments are difficult
  - A 'one-to-one' agreement should not be expected
  - **All models can be improved, this study aims to show where improvement is needed**
  - ***We make no statements of what is right or wrong, we just present the results***
  - *Even with the limitations of each of the current models, they are actually quite detailed and of high quality.*

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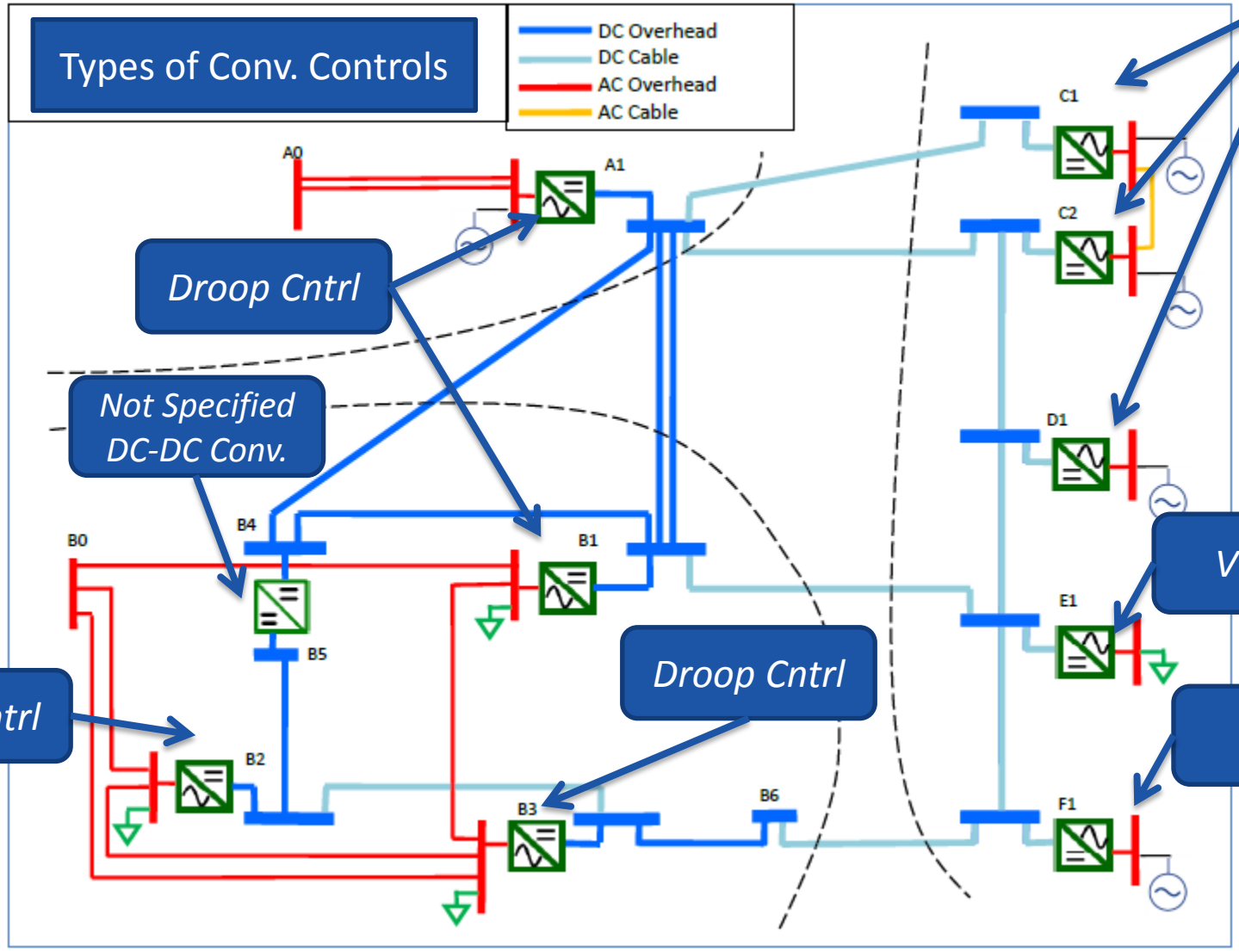
Outline

- Brief description of the models
  - Opal-RT (Matlab/Simulink + SimPowerSystems and eMegaSim from Opal-RT)
  - PSCAD from Manitoba HVDC Research Center
  - EMTP-RV from PowerSys and EMTP DCG
- Models differences
- Simulation Studies
  - Description and aim of the simulation studies
  - Selected results (all results available for scrutiny)
- General simulation challenges when using the benchmark models
- Recommendations and Further Work

Brief Description of the Models – Cigre DC Grid Test System



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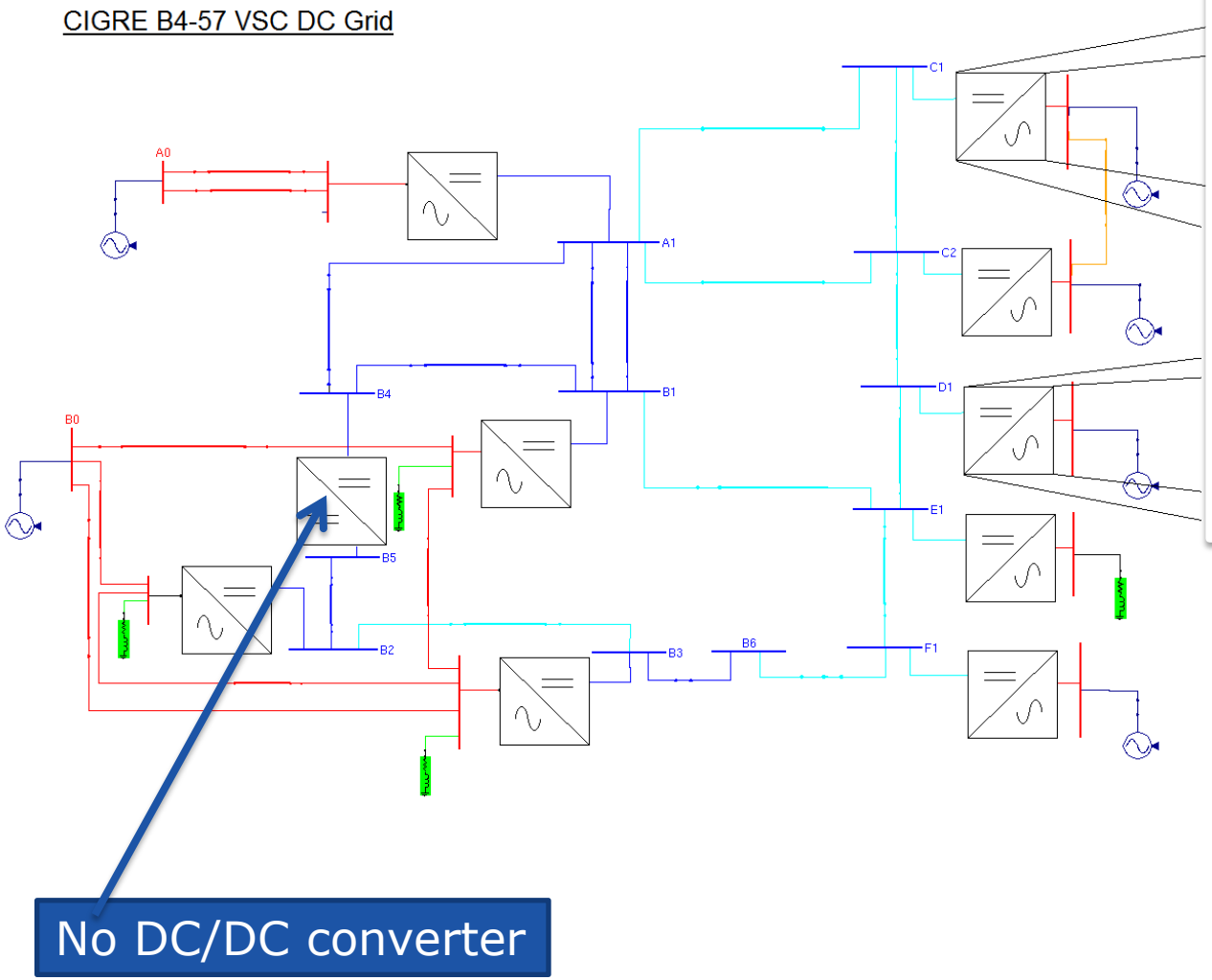
Test System in Opal-RT
(Layout from Hypersim)



Embedded VBE model means that the detail MMC cell model is implemented but without the cell capacitor balancing control (see the OPAL-RT presentation)

No DC/DC converter

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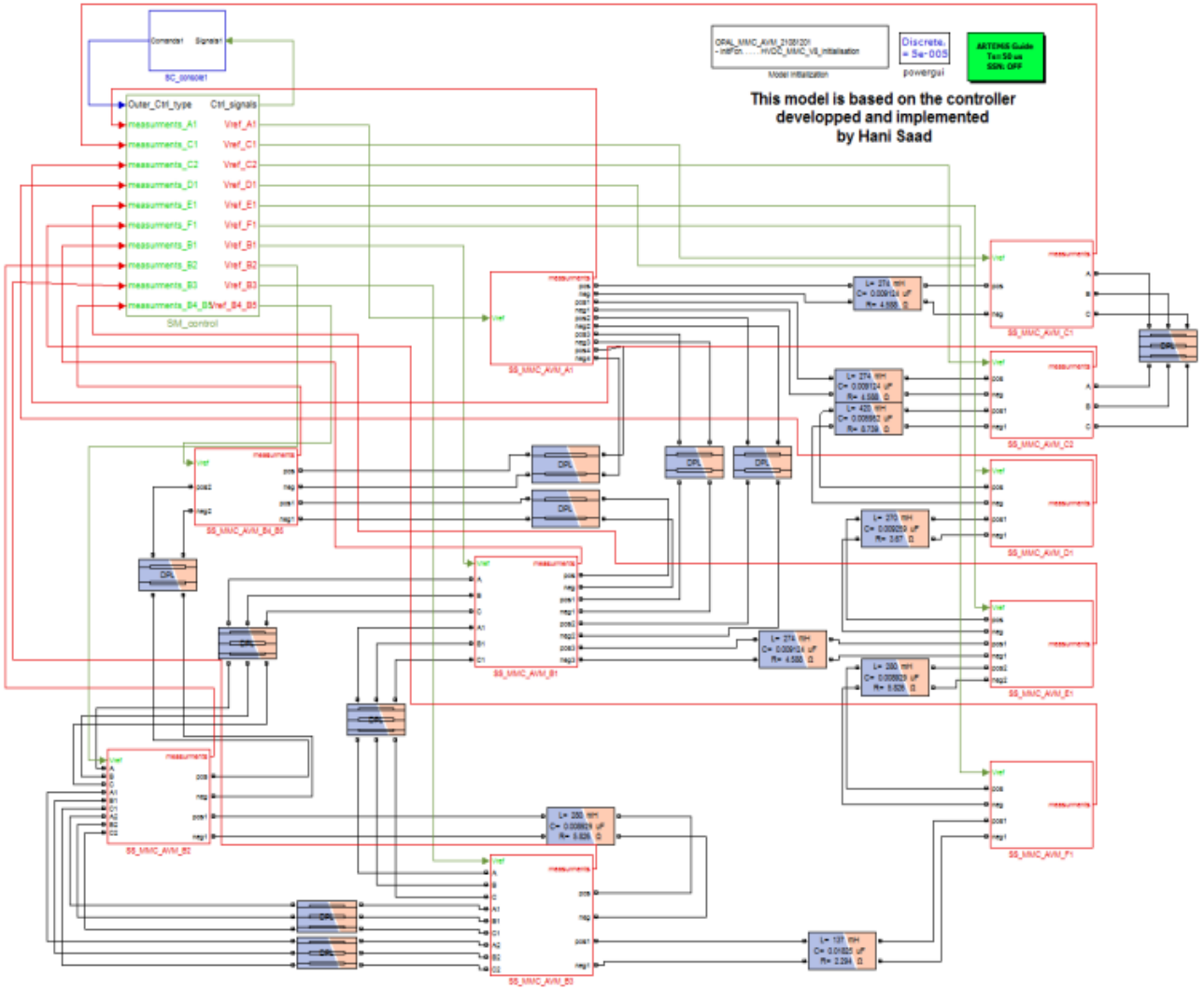
Test System in Opal-RT

(Top level model)



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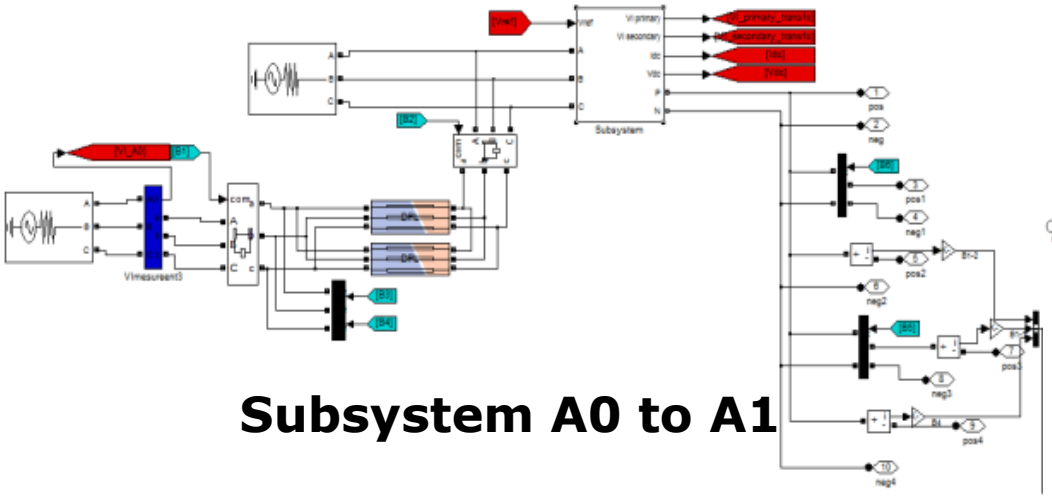
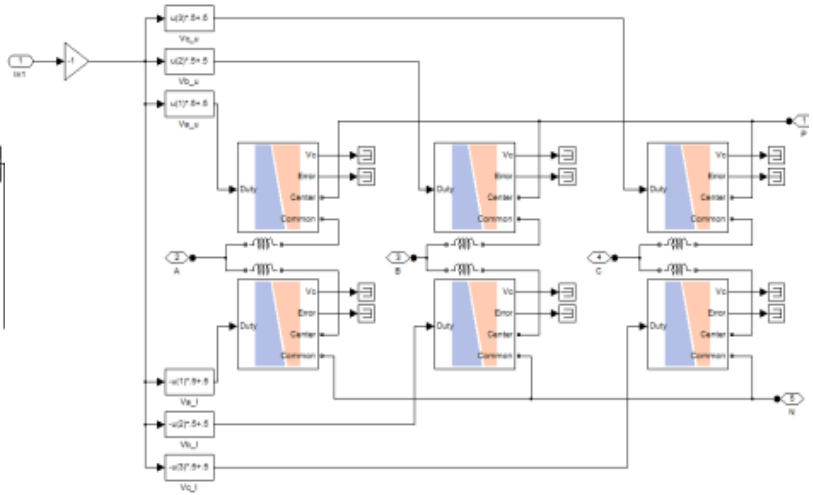
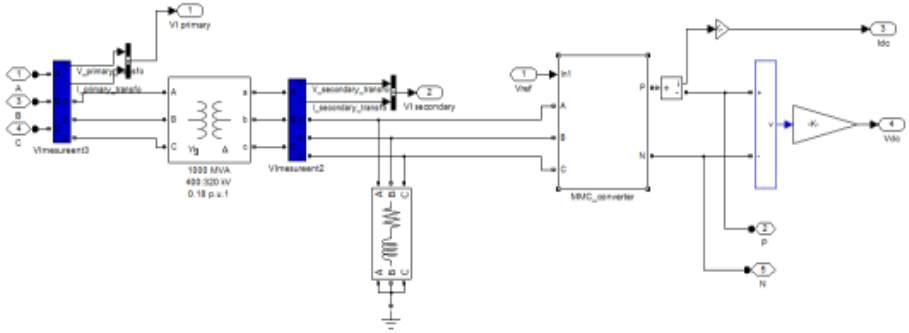
Test System in Opal-RT
(Subsystems)



Subsystem A0 to A1



MMC Converter



Subsystem of A1

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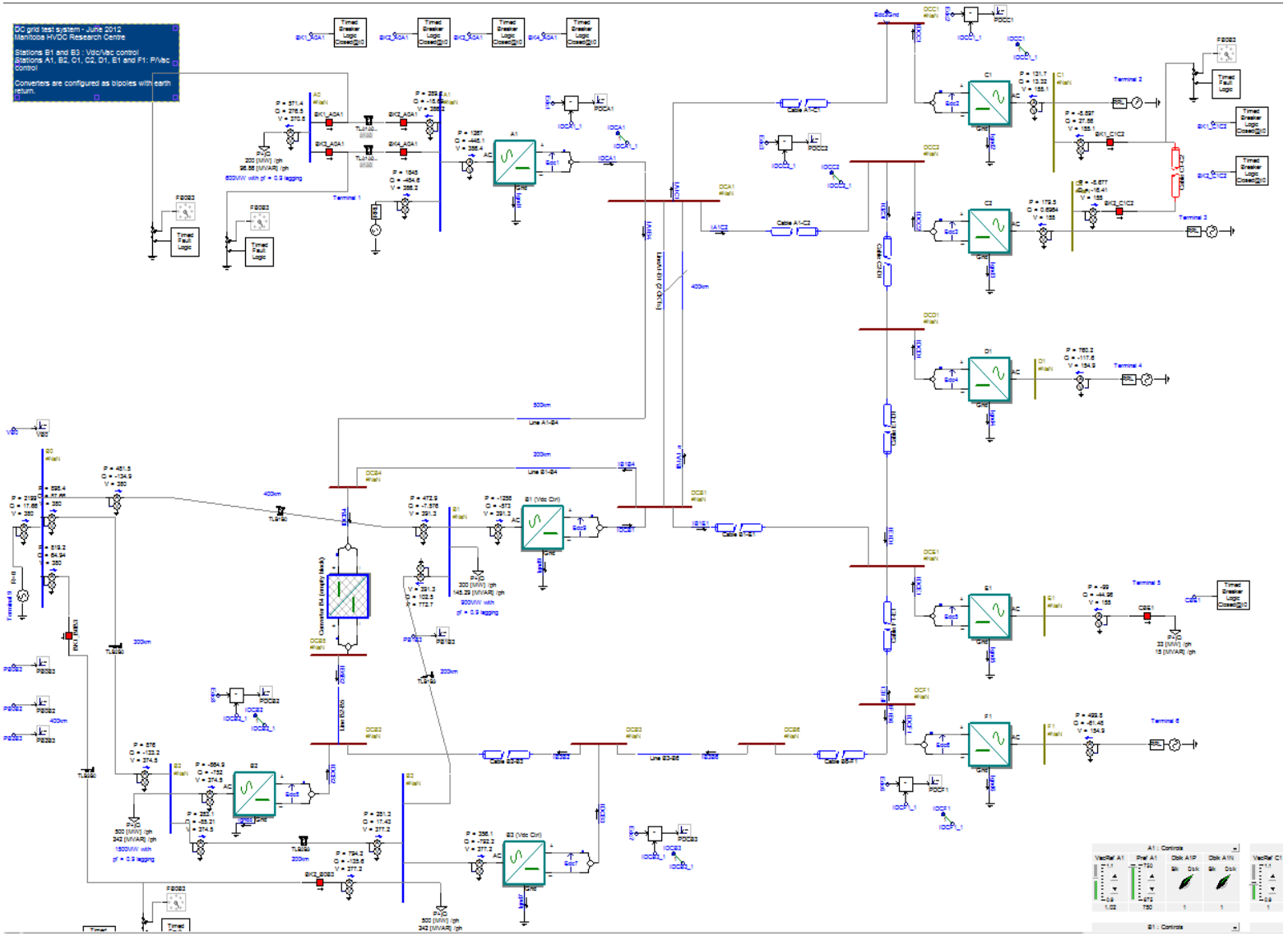
Test System in PSCAD



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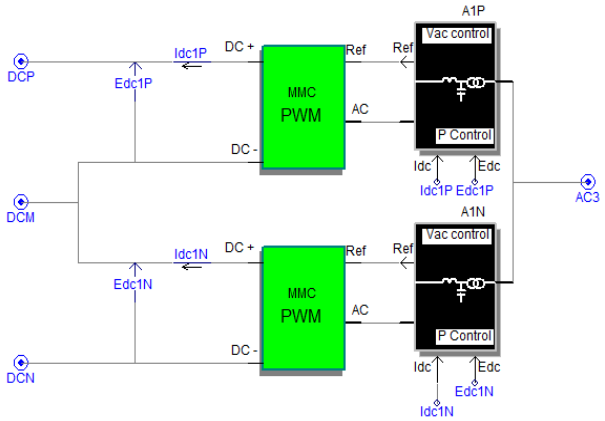
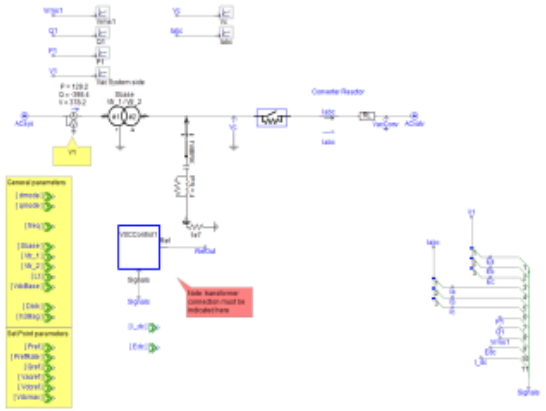
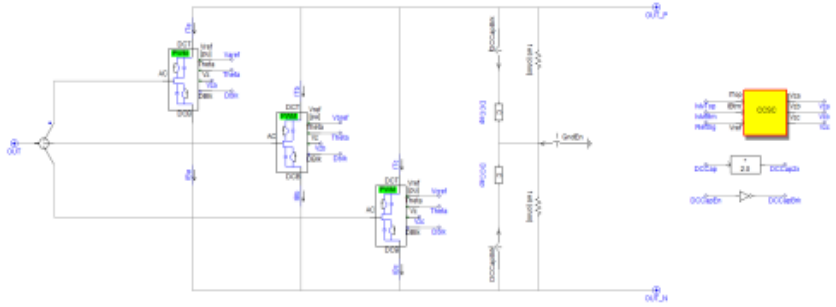
Test System in PSCAD



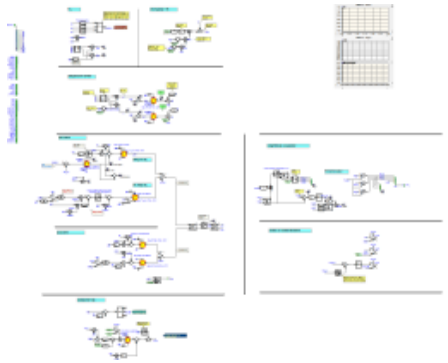
Converter A1



Converter controller



MMC PWM



VSC control

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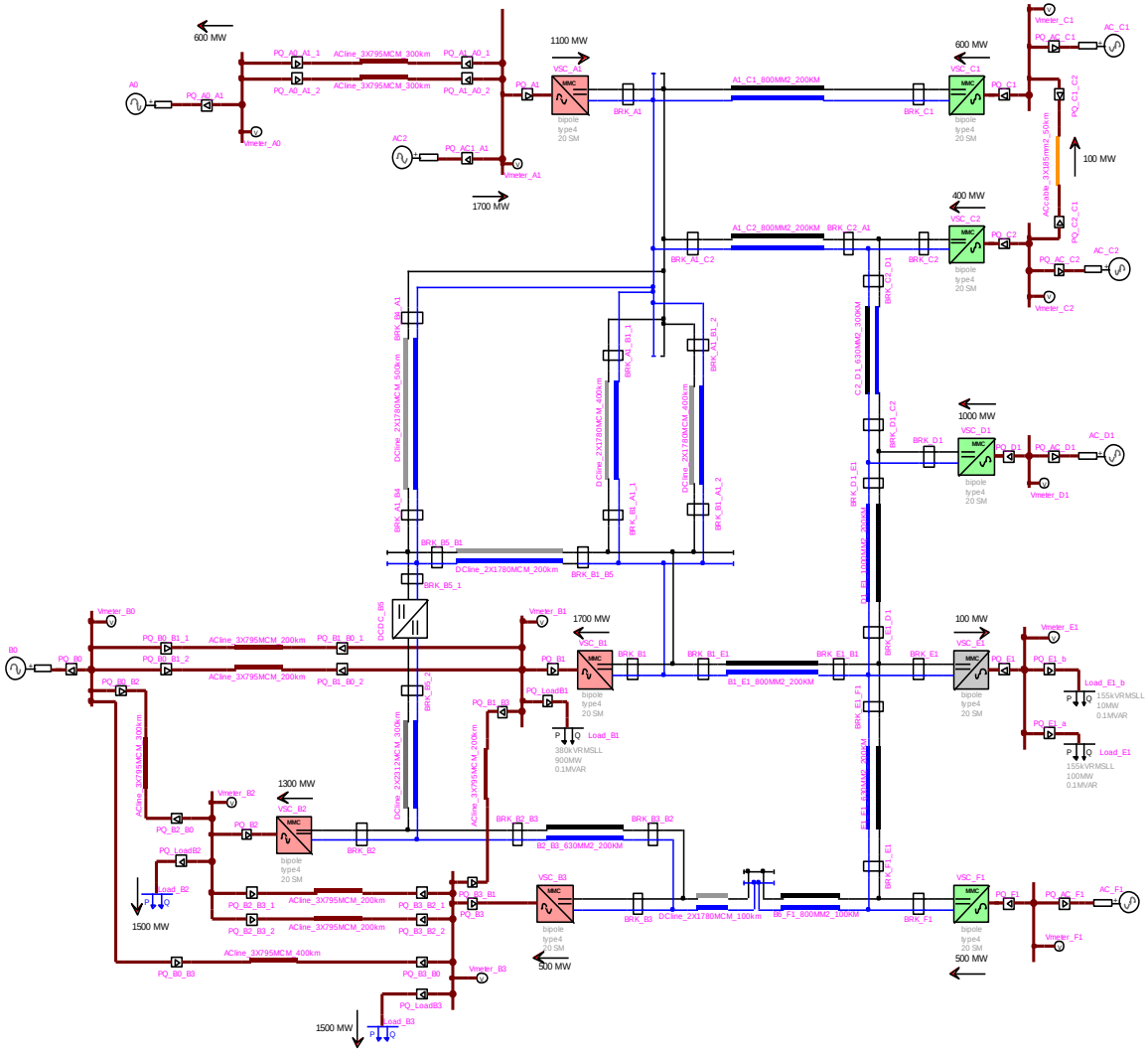
Test System in EMTP-RV



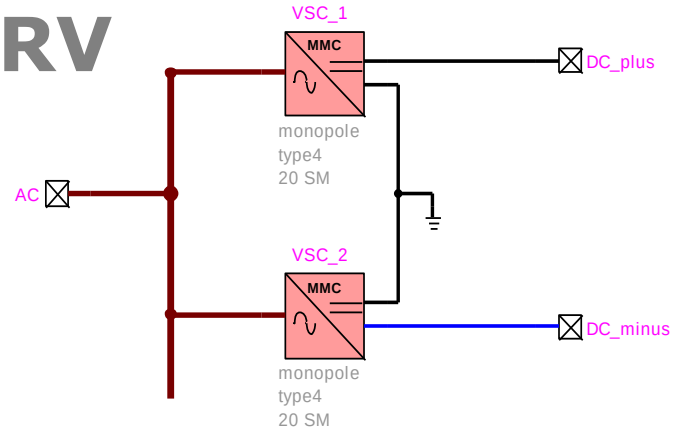
Double click to select the test case

→ Test case selection

Testcases 1 & 2

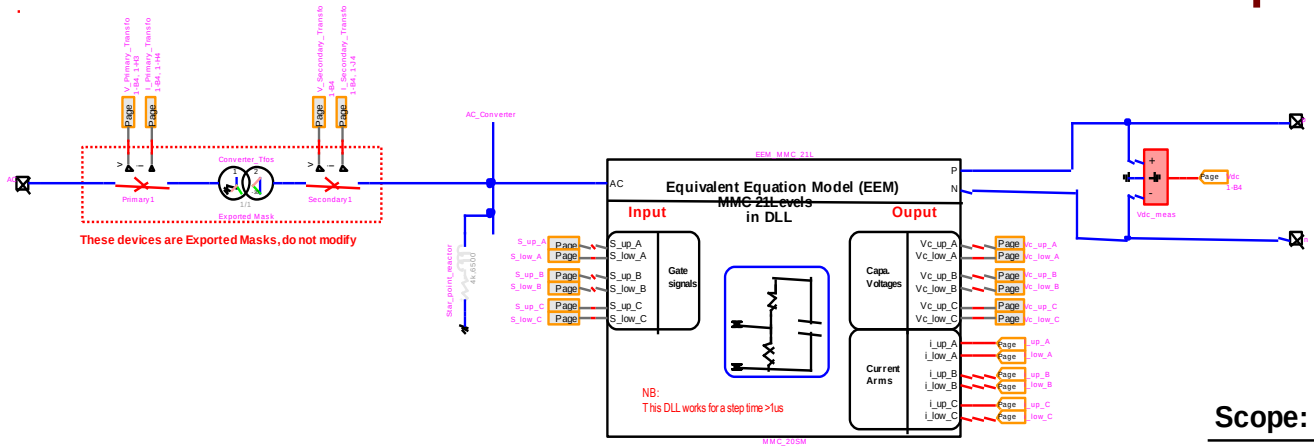
1. Steady state solution
2. Steady State Power Through Converters
3. Fault on AC grid
   - 3.1. Line opening
     - 3.1.1. Trip and reclose of Line 1: A0_A1_2 – A1_A0_2
     - 3.1.2. Trip and reclose of Line 2: B0_B3 – B3_B0
     - 3.1.3. Trip and reclose of Line 3: C2_C1
   - 3.2. Balanced 3 phase faults:
     - 3.2.1. Fault on Line 1: A0_A1_2 – A1_A0_2
     - 3.2.2. Fault on Line 2: B0_B3 – B3_B0
     - 3.2.3. Fault on Line 3: C2_C1
   - 3.3. Unbalanced 3 phase faults:
     - 3.3.1. Fault on Line 1: A0_A1_2 – A1_A0_2
     - 3.3.2. Fault on Line 2: B0_B3 – B3_B0
     - 3.3.3. Fault on Line 3: C2_C1
4. Response due to reference changes:
   - 4.1. Change in Pref at VSC_A1 (Droop Control): from 0.73 to 0.63
   - 4.2. Change in Pref at VSC_B2 (Droop Control): form -1 to -0.9
   - 4.3. Change in Pref at VSC_C1 (P control): from 1 to 0.9
   - 4.4. Change in Pref at VSC_F1 (P control): from 1 to 0.9
   - 4.5. Change in Pref at VSC_E1 (VF control): from -1 to -0.9
   - 4.6. Change in Vref at B2 (Vf control): from 1 to 1.02
5. DC Faults
   - 5.1. Trip and reclose of Line 1: A1_B1_1 – B1_A1_1
   - 5.2. Trip and reclose of Line 2: B5_B1 – B1_B5
   - 5.3. Trip and reclose of Line 3: B2_B3 – B3_B2
   - 5.4. Trip and reclose of Line 4: A1_C2 – C2_A1

Test System in EMTP-RV

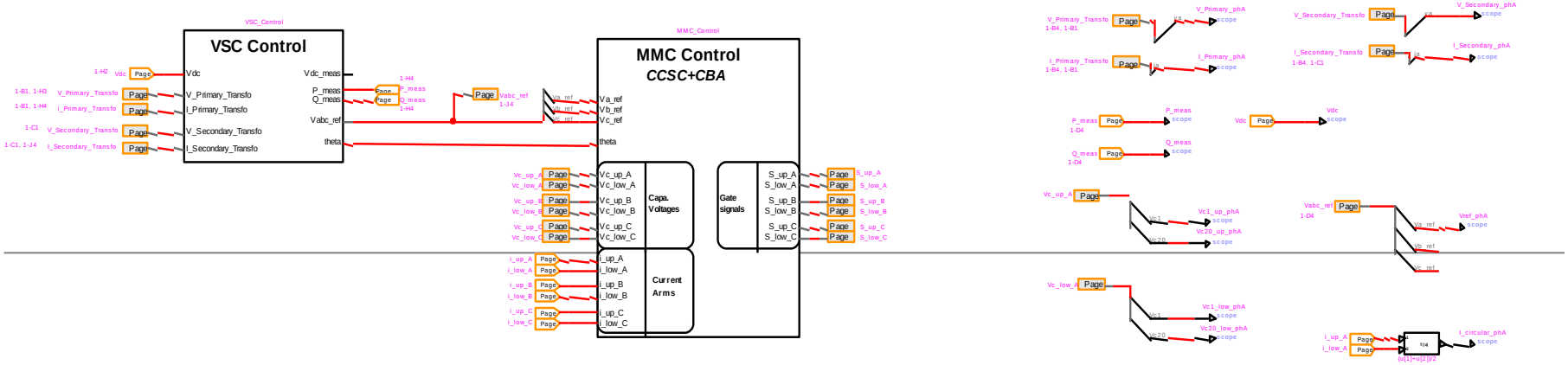


Converter A1

VSC_1



Scope:



Main Model Differences

- Opal-RT Model (Matlab/Simulink/SPS + Opal-RT Libraries)
  - Developed by Opal-RT (Luc-Angre Gregoire)
  - Embedded VBE for VSCs (Type 5 – see Opal-RT presentation)
  - No. of sub-modules per valve: two type of converters, 400 (for on-shore) and 20 (for offshore grid)
  - DC-DC Converter Model not included (B5 Converter)
  - 11 cores running in real-time with the eMegaSim simulator.
- PSCAD Model
  - Developed by Manitoba HVDC Research Center.
  - Detailed (equivalent Norton) models of VSC (Type 4 – all gate signals).
  - No. of sub-modules per valve: Two type of converters, one is 38 (MMC PWM) and the other is 98 (MMC)
  - DC-DC Converter Model not included (B5 Converter)
- EMTP-RV Model
  - Developed by RTE (Sebastien Dennetiere)
  - Detailed (equivalent Norton) models of VSCs (Type 4 – all gate signals).
  - No. of sub-modules per valve: 21
  - Type 2 (DM) also available.
  - Simplified DC-DC Converter **included**
  - *Documented modification from specification:* Parameters are modified in the AC side B0 and B1 line length is 200 km, 2 circuit lines (instead of 1 line of 400 km)
- Type 4 Definition
  - Reduction in each arm to limit the number of electrical nodes (based on the integration method – 1 arm, 1 equivalent)

Simulation Studies:
Steady State and Time Domain

- Simulation goals:
  - Determine the steady state performance of the test systems
  - Determine the dynamic performance of the test systems and terminals due to small perturbations, switching events (at DC), and faults (at AC)
- Simulation studies proposed (22):
  - Steady State Analysis (3)
  - Faults on AC Systems:
    - Line opening (3)
    - Balanced 3-phase faults (3)
    - Unbalanced 3-phase faults (3)
  - Response due to control reference changes
    - Perturbation in Pref at all controllers (5), Vref (1)
  - DC Faults: DC Line switching
    - DC line openings (4)
- Studies carried out: Opal-RT (21), PSCAD (16), EMTP-RV (22)
- Count: 59 simulations – 3 steady state, 56 time domain

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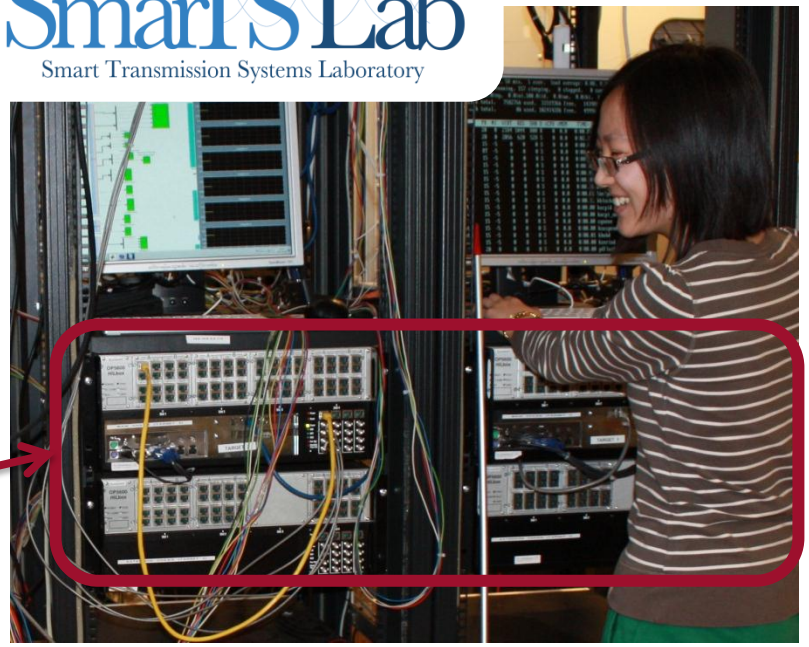
Model/User Limitations:

Simulations that could not be carried out

- Opal-RT
  - Change in Vref at DCDC_B5 (Simulation 4) Response due to reference changes
- PSCAD
  - Change in Pref at VSC_E1 (Simulation 4) Response due to reference changes
    - Model needs to be modified by adding a load at E1.
    - We ran out of time to do this.
  - Change in Vref at DCDC_B5 (Simulation 4) Response due to reference changes
    - Converter B5 is an empty block
  - All DC Faults
    - Could not figure out how to disable some internal breakers in the converters.
- EMTP-RV
  - All simulations were be executed.

Requirements to run the models

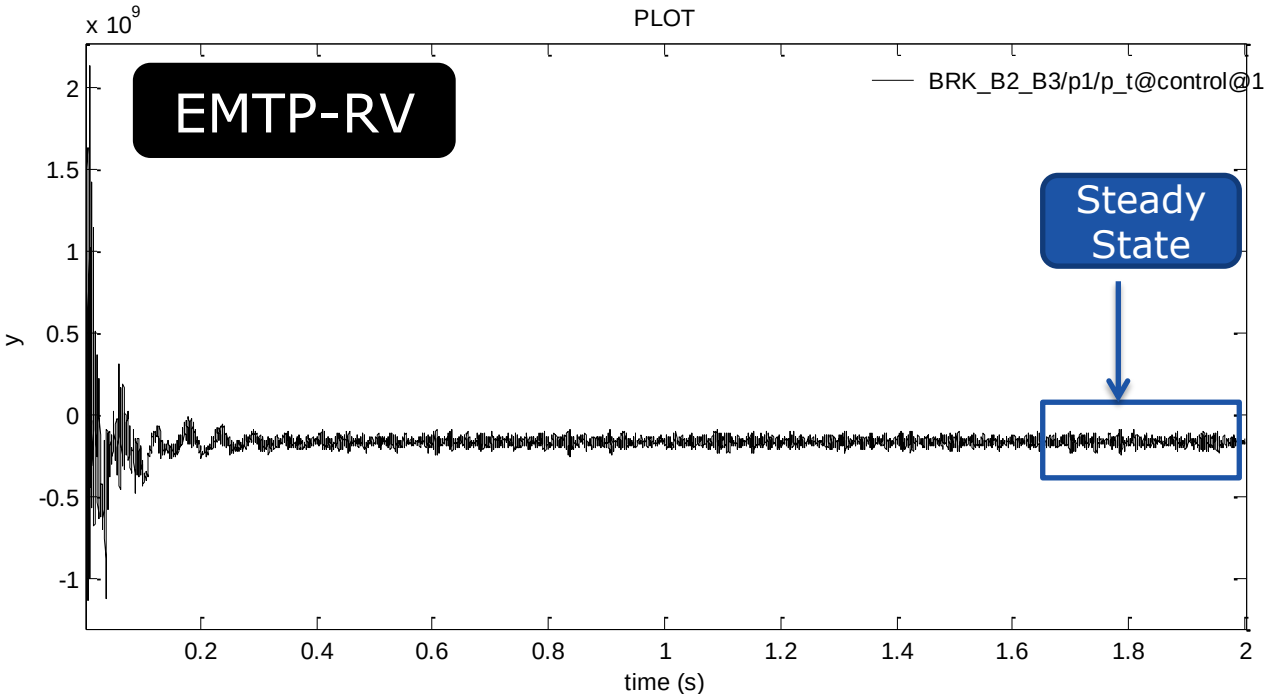


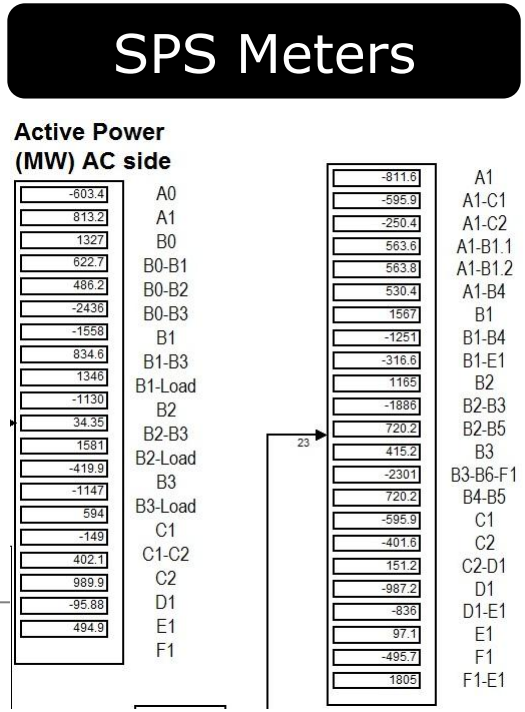
- Opal-RT
  - OPAL-RT real-time simulator ***OR*** license to run the compiled model in the PC (localhost license)
  - RT-Lab version 10.4.4.130, MATLAB Simulink 2011b (**32-bit**).
  - MMC libraries from Opal-RT
  - 11 processors

  (eMegaSim simulator at KTH SmarTS Lab has 24).
- PSCAD
  - Compiler: PSCAD requires a FORTRAN compiler. *In these simulation we use Intel® Visual Fortran Composer XE 2011* (v12) compiler (trial license).
  - Version of the software: PSCAD X4 (4.5.0.0) Professional edition (trial license).
  - Third party tools: If having the error of "WSock32.lib file missing", the Windows platform headers and libraries need to be installed by the users.
  - A VSC_MMC_lib file comes together with the model.
- EMTP-RV
  - EMTP-RV V2.4
  - MMC Toolbox
- ***FOR ALL OF THE ABOVE: PATIENCE!!!*** (and money…)

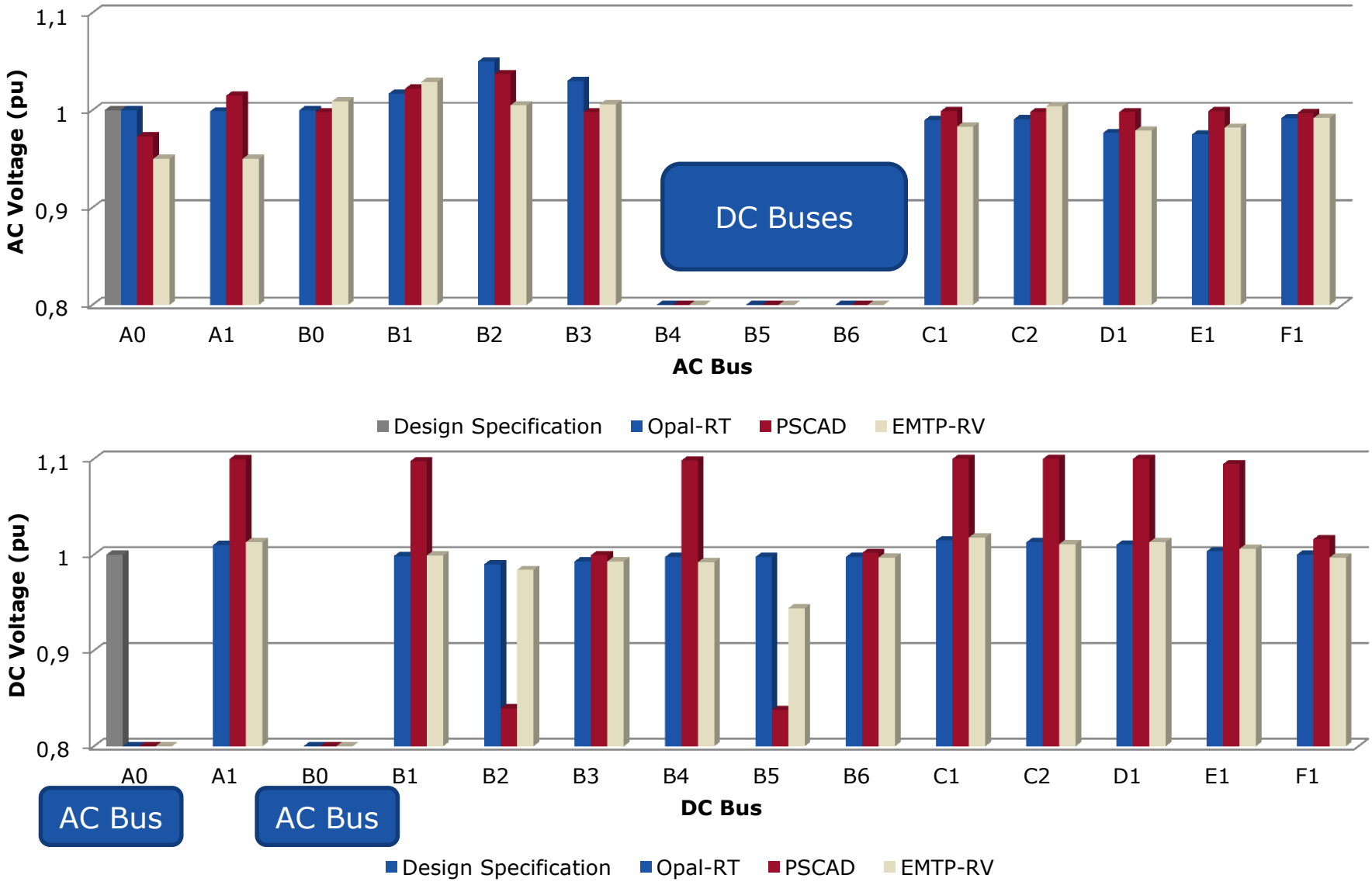
Steady State Analysis

- We consider the “harmonic steady state”, not power flow solution.
- Procedure: -run the simulation until it reaches a “steady state”
- Opal-RT and PSCAD models offer a “meter”.
- For EMTP-RV:

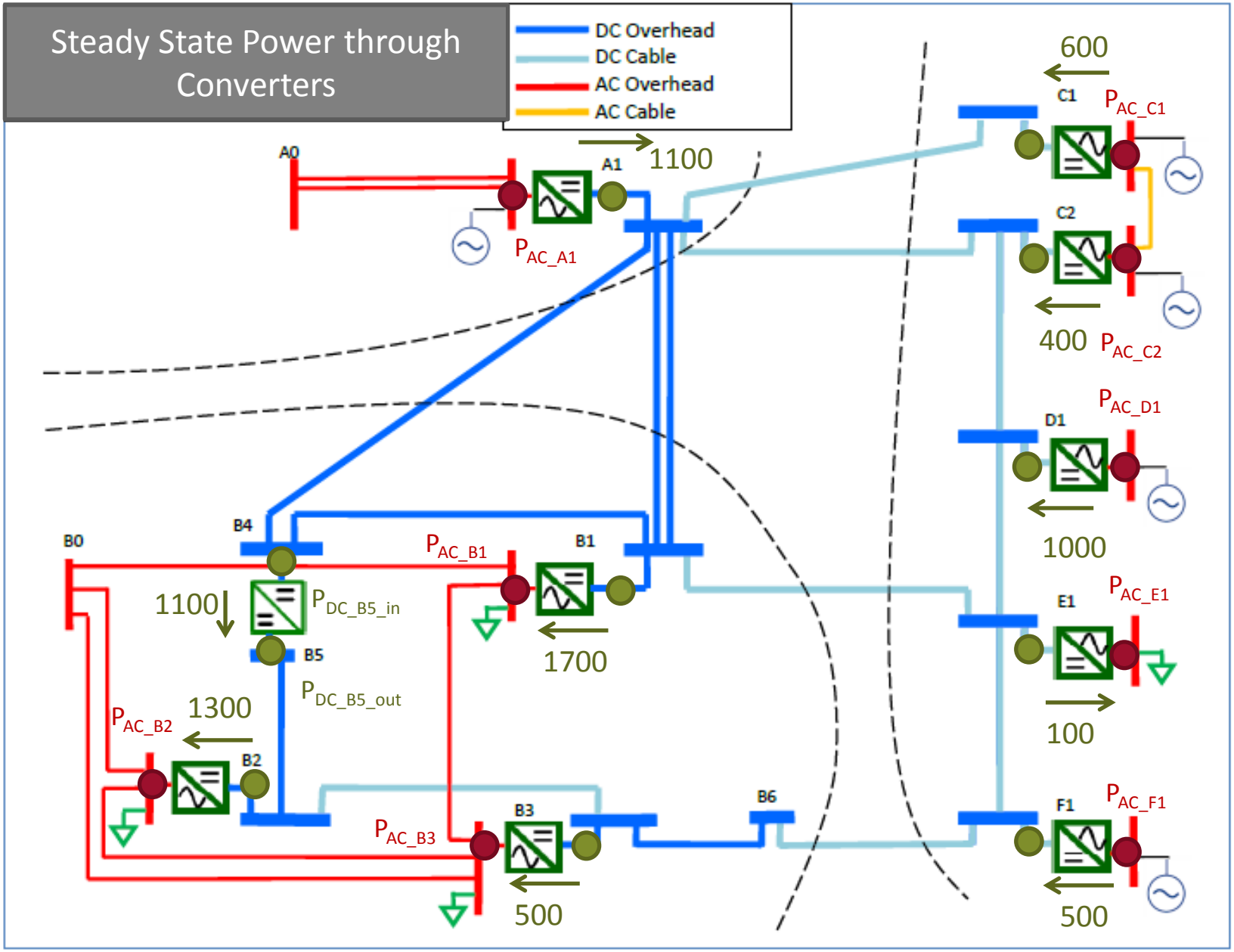




Steady State Solutions AC and DC Bus Voltages



Steady State Power Through Converters



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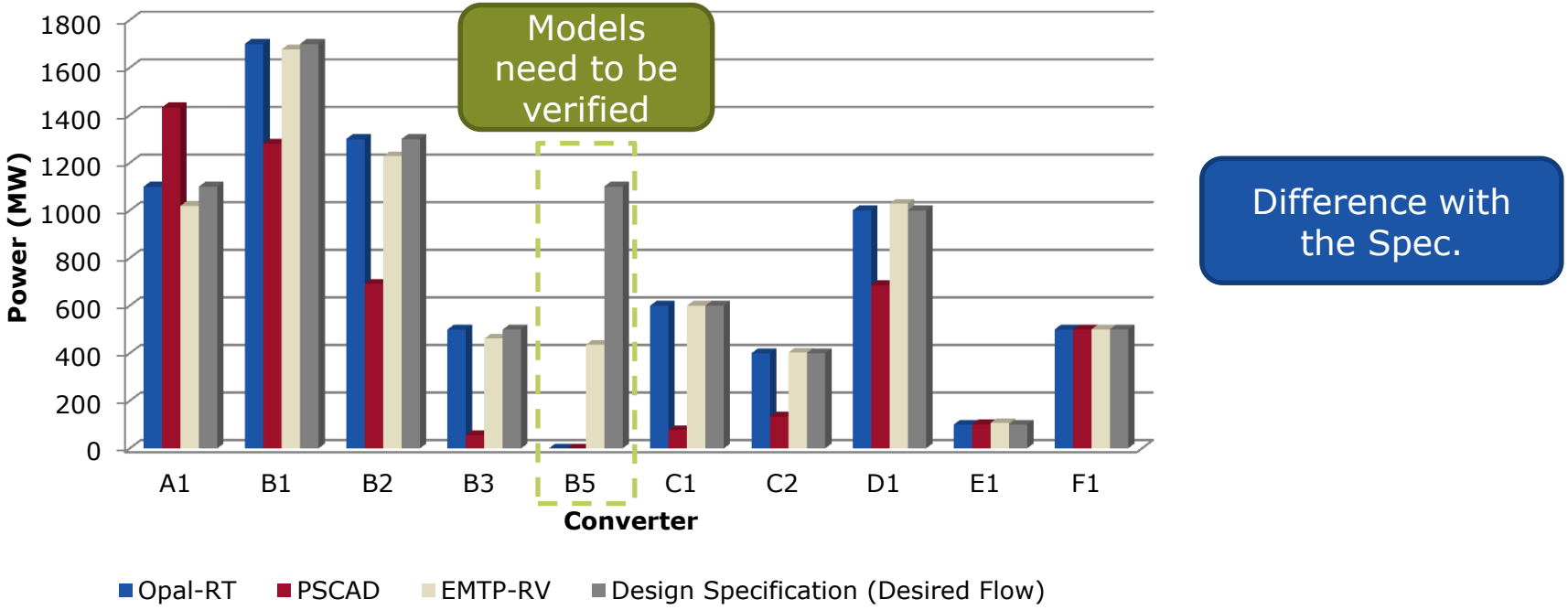
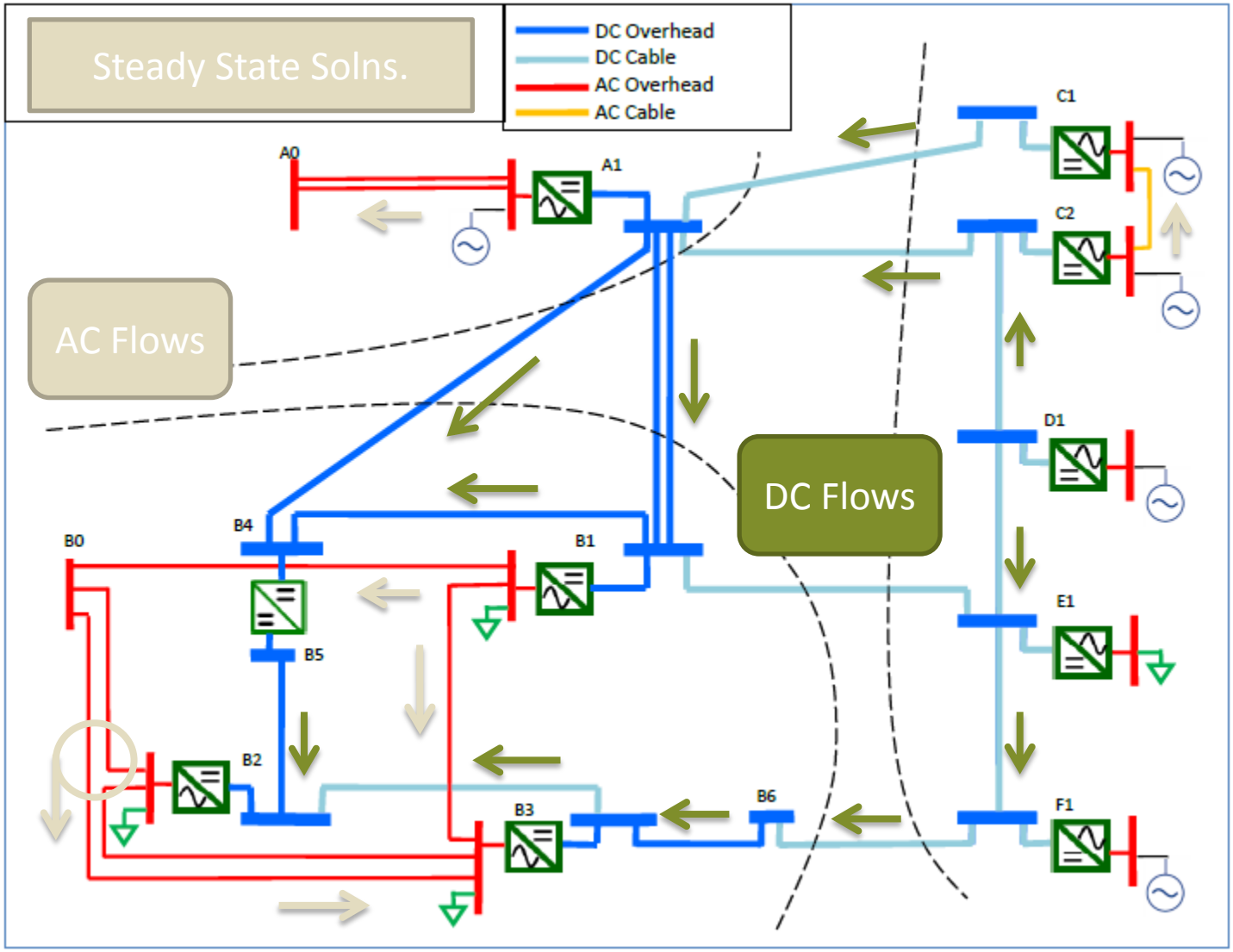
Comparison of Desired Flows: Design spec. with actual power through converters (max. value between input and output)



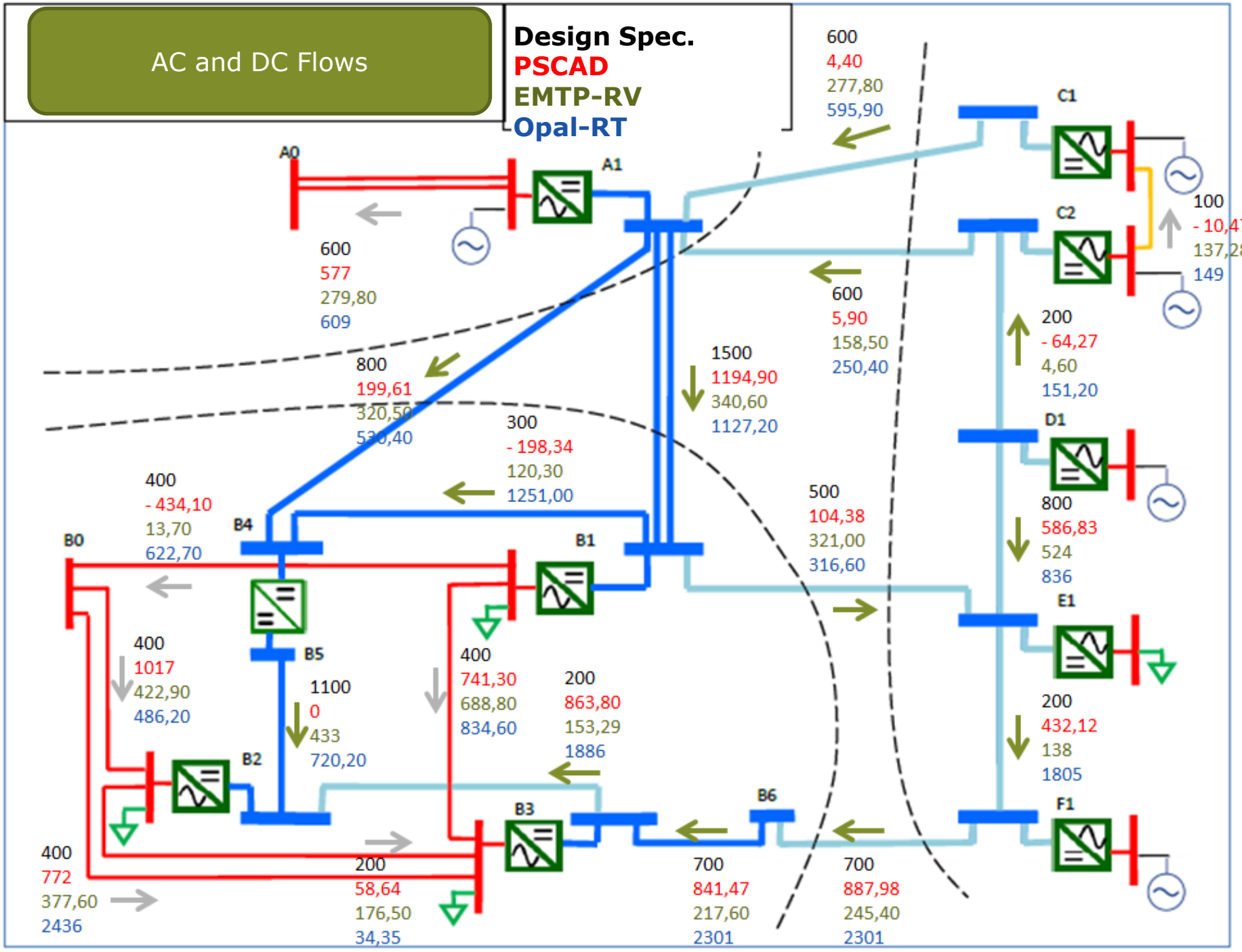
- The Opal-RT model matches the specification with no differences.
- There is a very reasonable agreement between the design specification EMTP-RV. Differences are likely due to tuning of model parameters.

Steady State Solutions
(Harmonic Steady State) – AC and DC Flows



AC and DC Flows

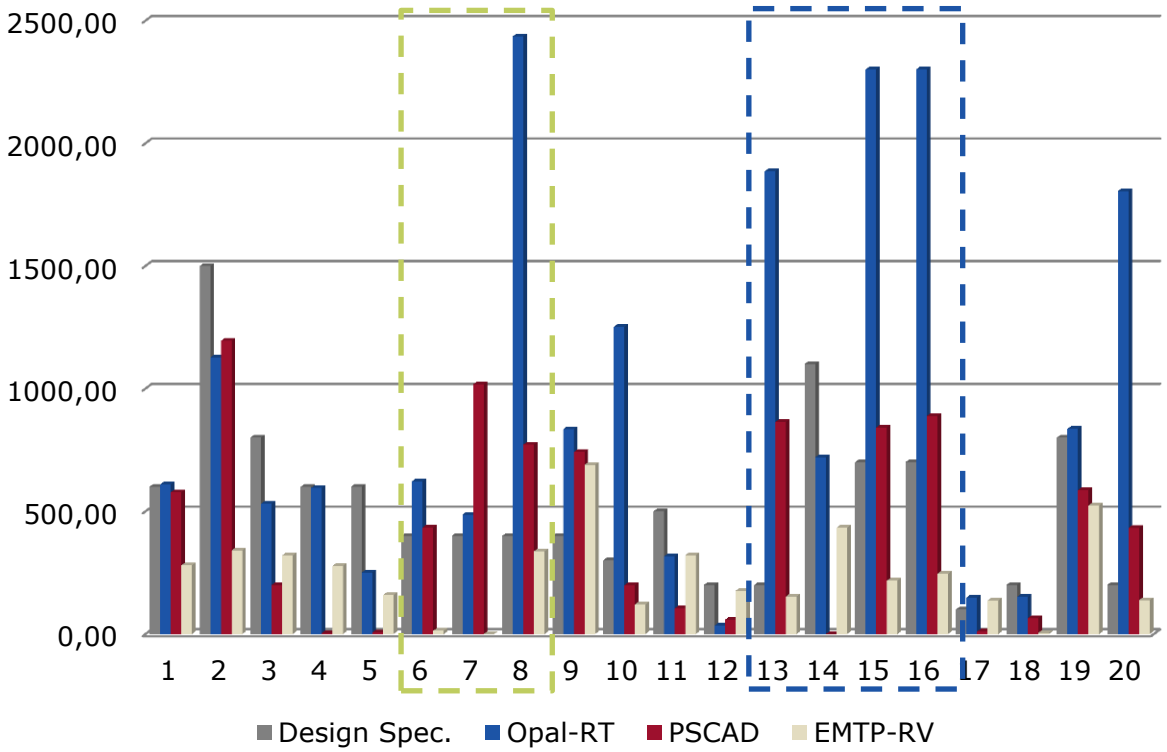
Design Spec.
PSCAD
EMTP-RV
Opal-RT



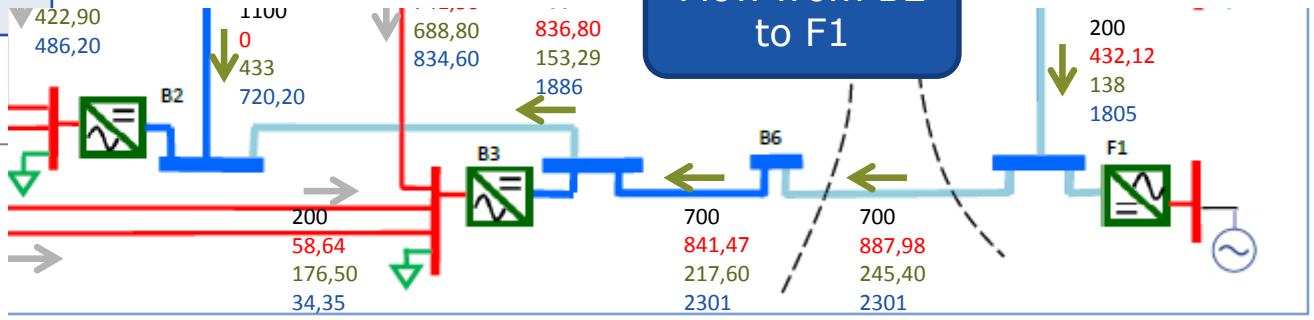
Results
Absolute Values Shown

Line no.	From Bus	To Bus	Design Spec.
1	A1ac	A0ac	600,00
2	A1dc	B1dc	1500,00
3	A1dc	B4dc	800,00
4	C1dc	A1dc	600,00
5	C2dc	A1dc	600,00
6	B0ac	B1ac	400,00
7	B0ac	B2ac	400,00
8	B0ac	B3ac	400,00
9	B1ac	B3ac	400,00
10	B4dc	B1dc	300,00
11	B1dc	E1dc	500,00
12	B2ac	B3ac	200,00
13	B3dc	B2dc	200,00
14	B5dc	B2dc	1100,00
15	B6dc	B3dc	700,00
16	F1dc	B6dc	700,00
17	C1ac	C2ac	100,00
18	C2dc	D1dc	200,00
19	D1dc	E1dc	800,00
20	E1dc	F1dc	200,00

Directly Connected to Slack Bus

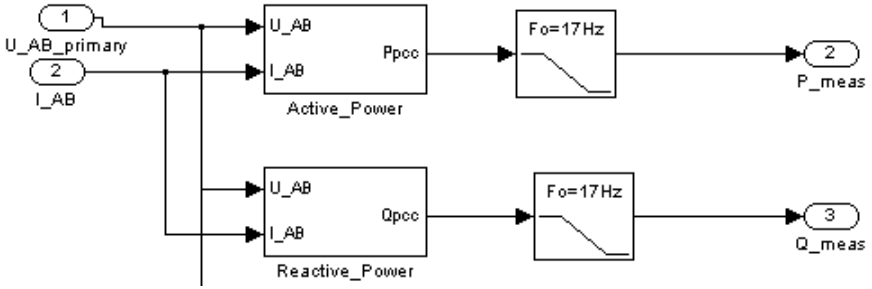


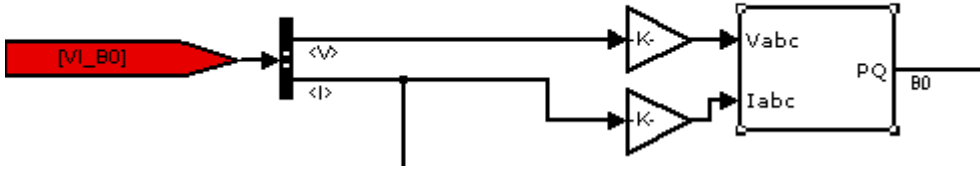
Flow from B2 to F1



Source of errors in power measurements in Opal-RT model

- In some of the AC measurement, the output was filtered after power computation. For the DC case, only the instantaneous power without filtering was used.





Also, the power in each AC line was deducted from the measurement of each converter. There is a lot of room for error in doing this way. Next version of the model should include more measurement to avoid such error.

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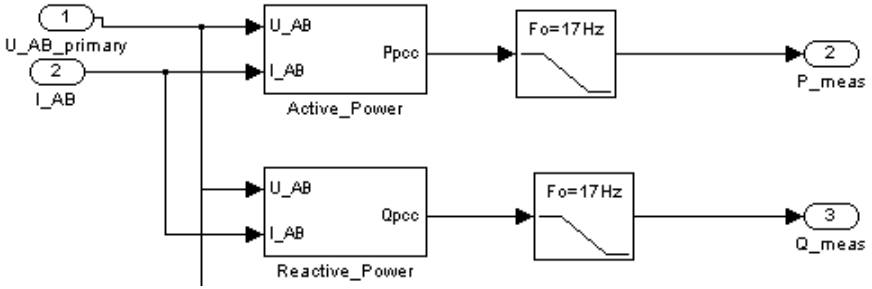

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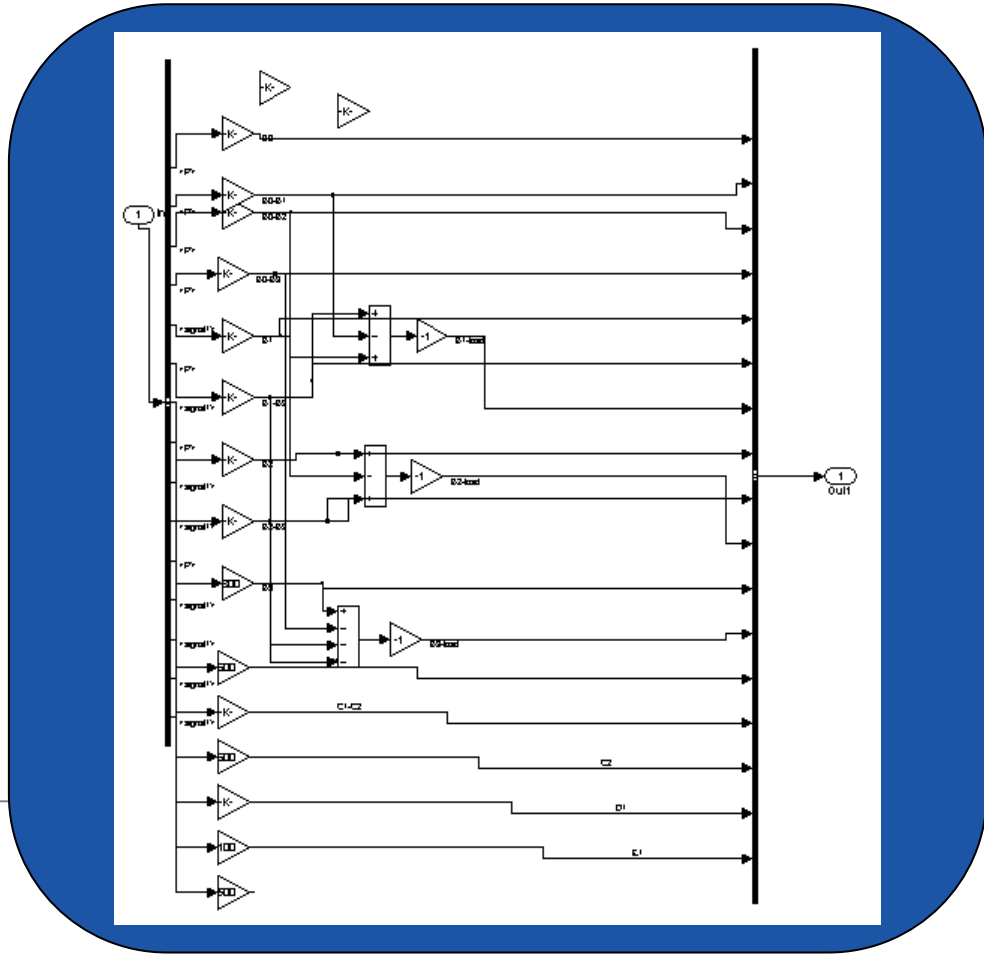

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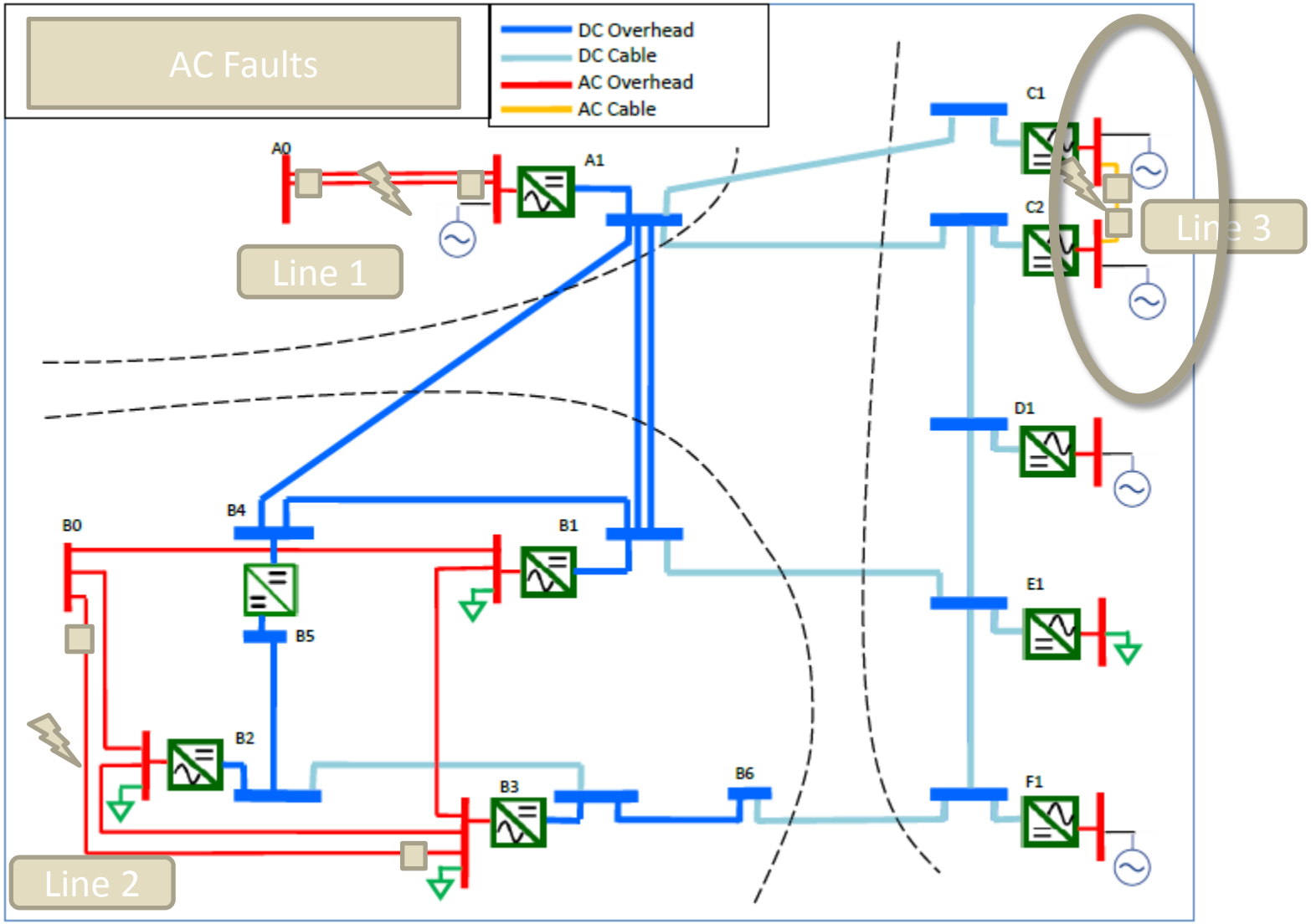
Faults on AC Systems



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Faults on AC Systems

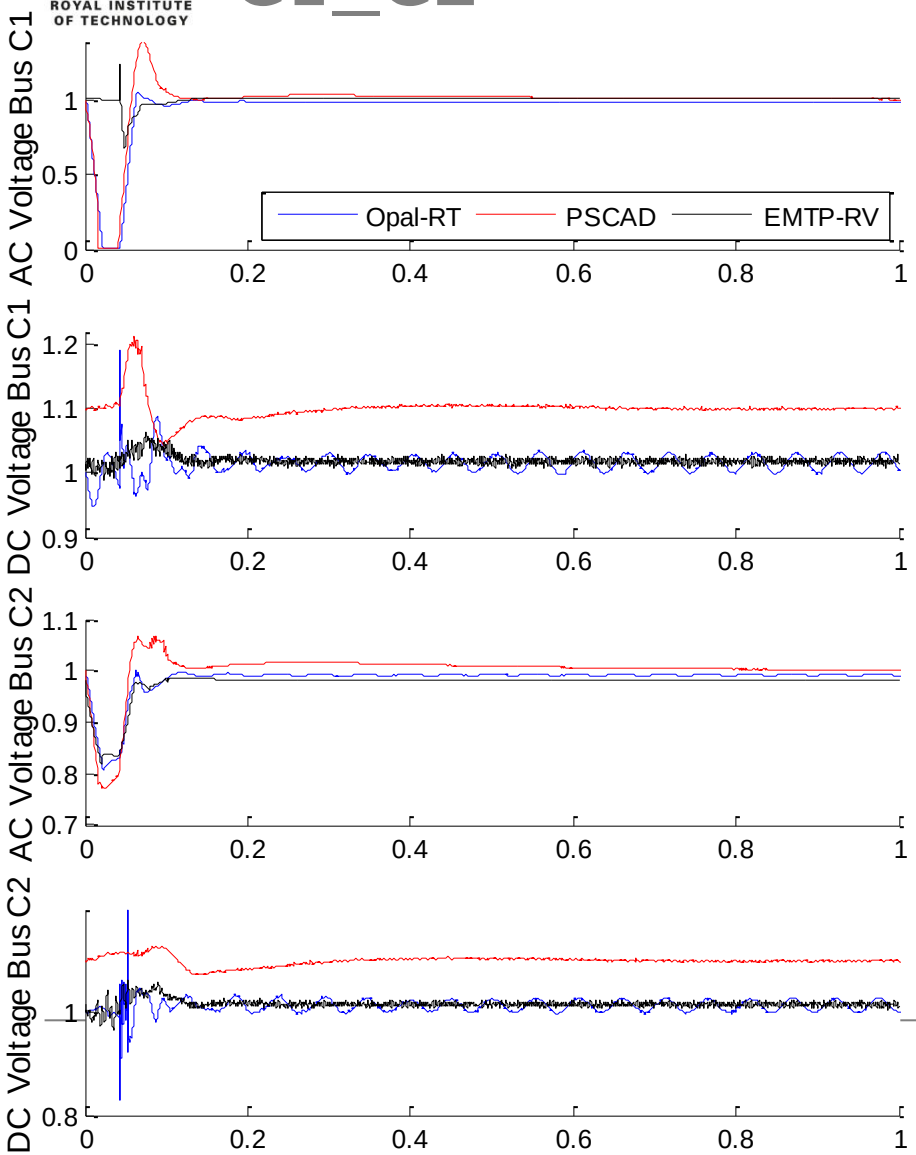
All changes applied at t=1 sec after harmonic steady state soln.

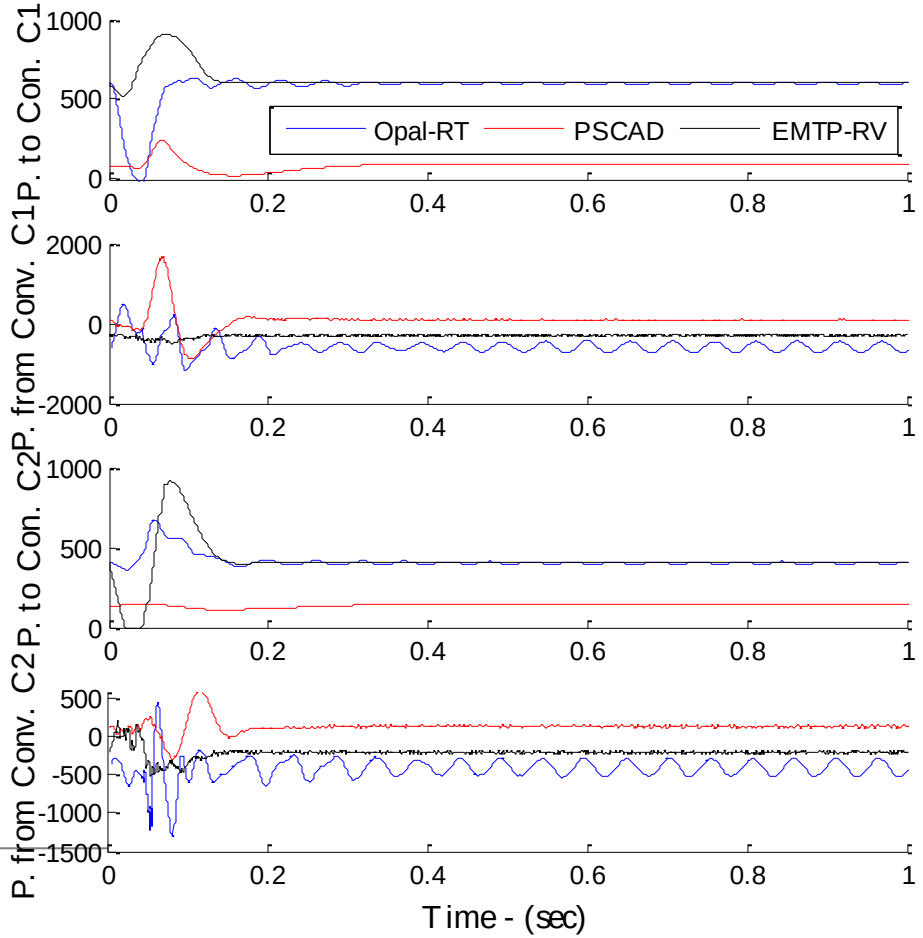
Balanced (3 phase) [or unbalanced] fault is applied at left-hand (or upper) side bus of the line.

Ideal AC breakers are placed on each side of the line.

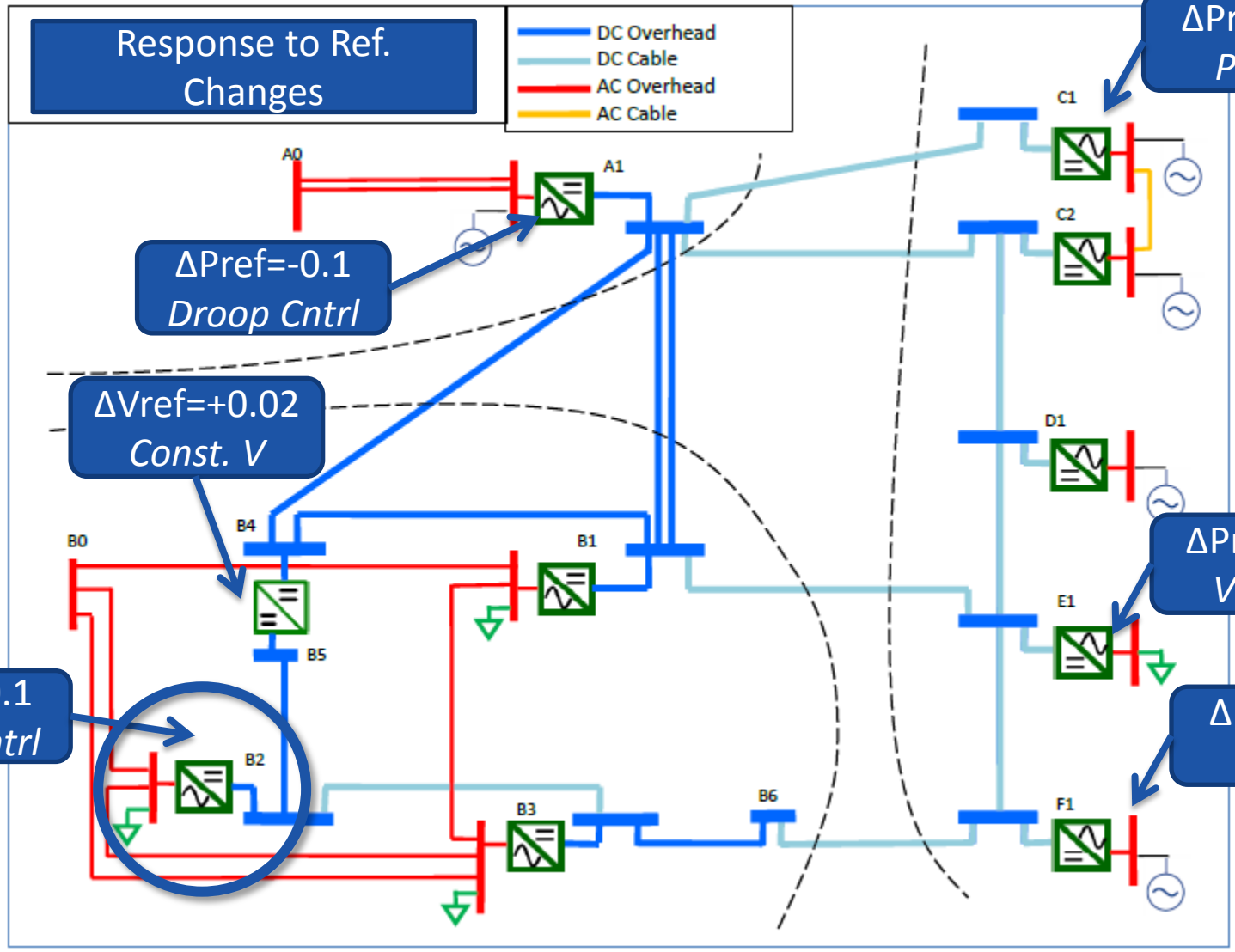
*The line is opened **after** 2 cycles (0.04sec), after this to cycles the fault is cleared by opening the breakers on left hand side and right hand side simultaneously, and closing them simultaneously after 2 cycles.*

Balanced Fault on Line 3: C1_C2





Response Due to Reference Changes



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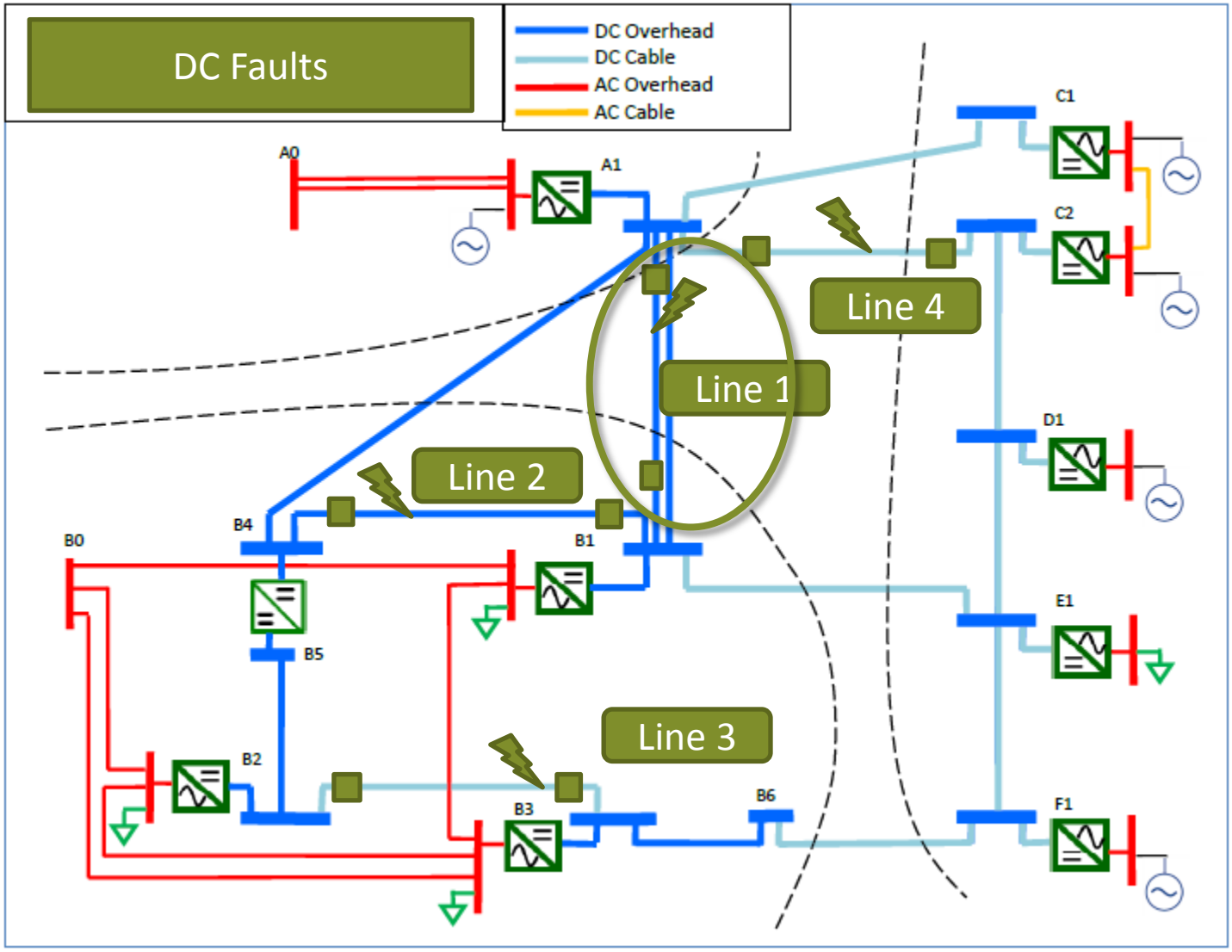
Faults on DC Grid



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General Simulation Challenges

- Opal-RT
  - Separate subsystems in order to run in real-time
  - Need a model compiler for the specific architecture of the system and software configuration.
  - Model modifications during real-time simuation
    - Con.: No possibilities of modifying the circuit model for real-time simulation, but ok for off-line (although this takes out the advantage of having an RT simulator)
    - Pros.:
      - Control parameters can be modified while real-time simulation is running.
      - RT simulator can be used in "Simulation Accelerator" mode when no I/O is used (faster than real-time)
  - Capacitor Balancing:
    - Detailed MMC cell model was used.
    - However, the DC voltage of each capacitor is adjusted to the average value of the sum of the cell capacitor voltage.
    - The capacitor voltage balancing control system is therefor not implemented (but available).

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General Simulation Challenges

- PSCAD
  - Errors that are difficult to figure out:
    - Example1:Component ‘***’ does not have a corresponding definition.
    - Solution: loading the library has to do before loading the model.
    - Example2: ***No rule to make target ‘***.mak’. Stop
    - Solution: install suitable compiler (GNU Fortran compiler is not suitable)

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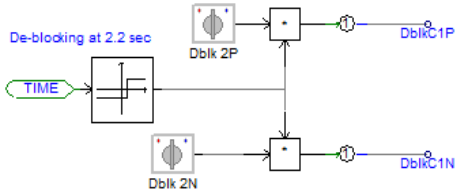
- PSCAD
  - **Aspects not documented that make it difficult to use the model**
    - In link tab of project setting, the user must manually add these sub-directories to the directory specified by the User Library Path input in the Workspace dialog. In this simulation, we need to choose ‘if12 (Intel Visual Fortran compiler versions 12)’.
    - De-blocking the converter control for several seconds at the beginning of the simulation, which is not indicated when providing this model.

Converter name	E1	B1	A1	C1	C2	D1	B2	F1
De-blocking time(s)	1.5	0.2	2.4	2.2	2.0	0.6	0.8	1.7



    - Some newly developed components do not have help information. For example, the DC breaker.

General Performance Observed (ONE Specific Case)

A. Simulation "t" to reach a steady state
B. Time effort to carry out one simulation

- **Opal-RT (50 µsec time step)**
  A. Approximately 1 sec
  B. Simulation time: Real time. (1 sec. = 1 sec.)

- **PSCAD (20 µsec time step)**
  A. Approximately 5 sec
  B. Simulation time: about 1 hr for a 15s simulation
  (Initialization Work Around - if system is left unchanged: start from a snapshot (snapshot for initialization)

- **EMTP-RV (40 µsec time step)**
  A. Approximately 0.5 sec.
  B. Simulation time: 258.625 sec for 2 second simulation.

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Recommendations and Further Work

- The three models simulated are very complex and detailed, and will certainly be useful for DC Grid studies.
- We make the following recommendations for improvements on the current models!
- **Documentation:**
  - Currently the EMTP-RV and SPS models are designed only for the scenarios presented.
  - Documentation on the models (details) are needed for preparing other studies.
- **Model Harmonization:**
  - The DC Grid benchmark models need to:
    - Be harmonized in terms of steady state solution
    - Controller implementation should be identical
  - For large DC Grid studies, the focus is not on converter performance, and detailed representation of the VSCs might be unnecessary
    - The use of a common average value model for the VSC is recommended, but this must be validated with detailed models
    - (Detailed models are only necessary for internal protection and performance analysis)

Recommendations and Further Work

- **Validation:**
  - Component validation
    - Validation *across different simulation environments* should start at the component level for comparison studies to be meaningful:
      - Controller validation should be first (check controller response to isolated inputs – compare outputs)
      - VSC validation (for AVM), DC Line models and breaker models
      - Independent validation of AC grid portions
    - Component level validation with "real" measurements would be AWESOME!
      - Some suppliers and R&D centers have comparisons with actual hardware or analog set ups, but it is not public.
  - Point-to-point DC Link:
    - Validation is recommended to establish the core differences of a simple DC Grid operation under different control modes in the three different environments.

Recommendations

Looking into the Future: Avoid Modeling Ambiguity

- *Modeling and Simulation without Ambiguity!*
- The efforts in developing these benchmark models is of great value for DC Grid development.

- However, DC Grid development will be hindered due to a lack of ability:
  - To share (validated) models across different simulation environments.
  - Which in turns requires the re-implementation of models in different tolls (very costly!).
  - In this case models need to be validated.

- This study has shown that there is a clear ***need for unambiguous model exchange***
  - Model exchange not referring only to parameter data
  - Actual model implementations differ: "what's inside the box?" is not transparent to the user
  - Challenge for users without access to all software (economically prohibitive)

- This problem has existed since about 40 years for conventional AC/DC system design! (J. Belanger)
  - DC Grid development should strive to tackle this attitude for common benefit.

Recommendations – Looking into the Future: Avoid Modeling Ambiguity

- **Possible solutions to ambiguity**
- Modelica-based models:
  - Modelica is an OOP modeling language for complex systems
  - Modelica models allow the specification of *both* the model equations and parameters
  - A DC Grid model could be entirely defined, without ambiguity, and shared.
  - Files could be packaged so that the model inside remains "closed".

  - Caveat: Each simulation environment needs to translate from Modelica to their internal definition (which requires validation). Mapping to GUI, etc…

  - However:
  - The use of Modelica language for **very large** AC/DC networks still need to be demonstrated. FP7 Pegase project had very promising results for moderate size networks.
  - Usually, network solution used specialized circuit solvers (nodal …) with system topologies and component parameters. Are topology-based specialized solvers available in Modelica?

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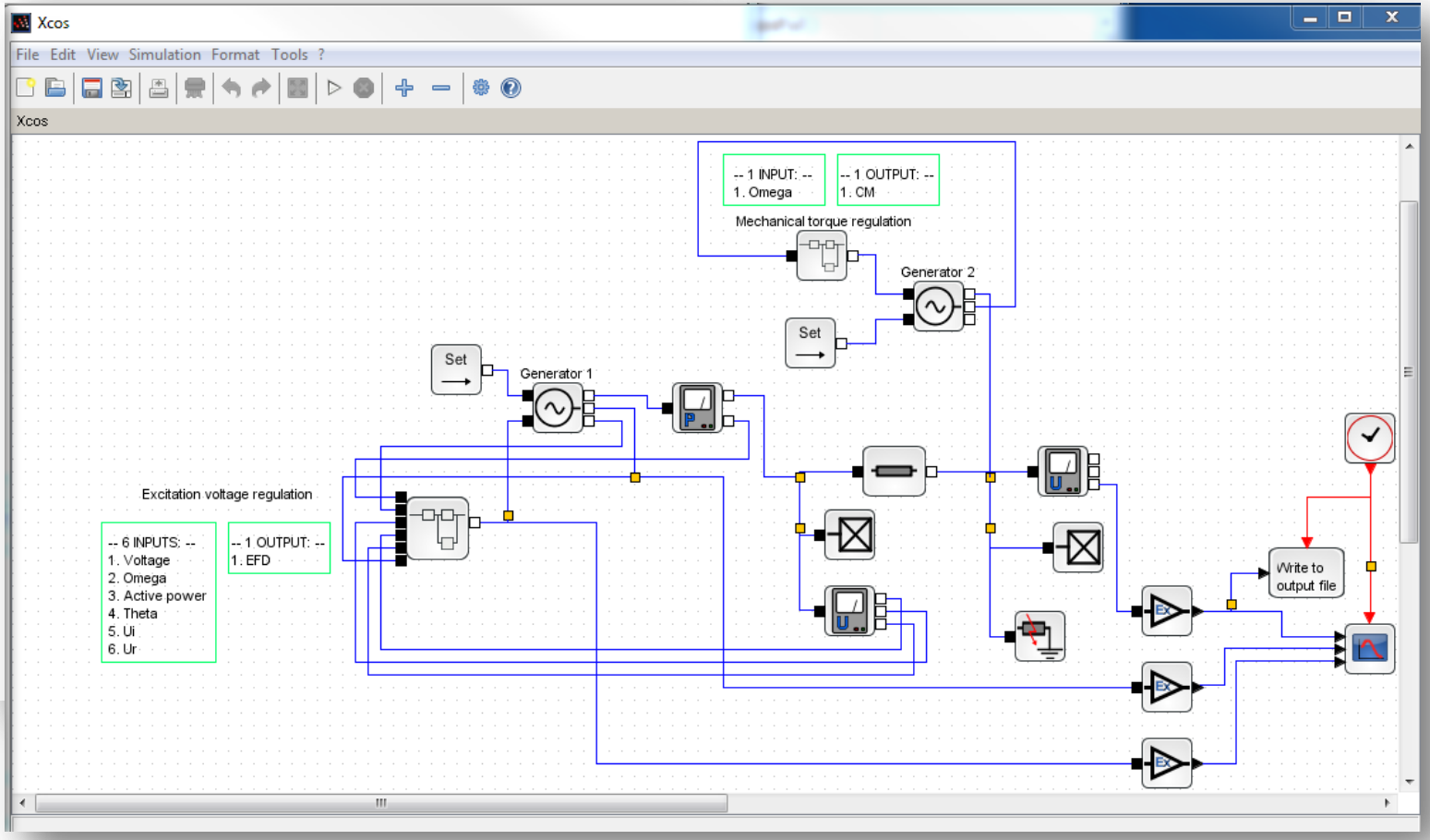
Proof of concept:

Sharing Modelica Power System Models in two different simulation environments



Simulation results in Scilab/Xcos and Dymola, respectively. They are absolutely the same.

Courtesy of Wei Li (KTH), Angela Chie and Patrik Panciatici (RTE)

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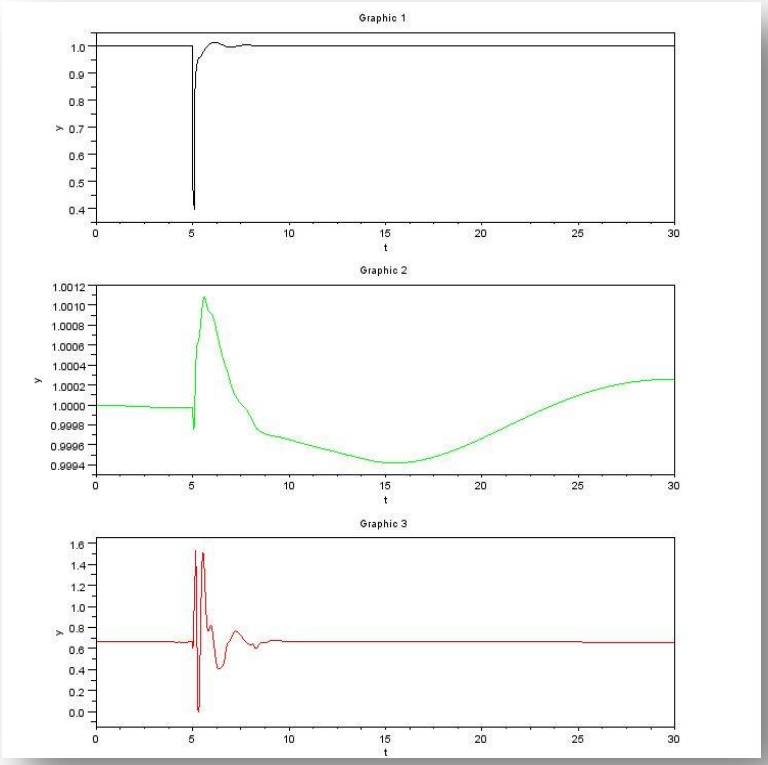

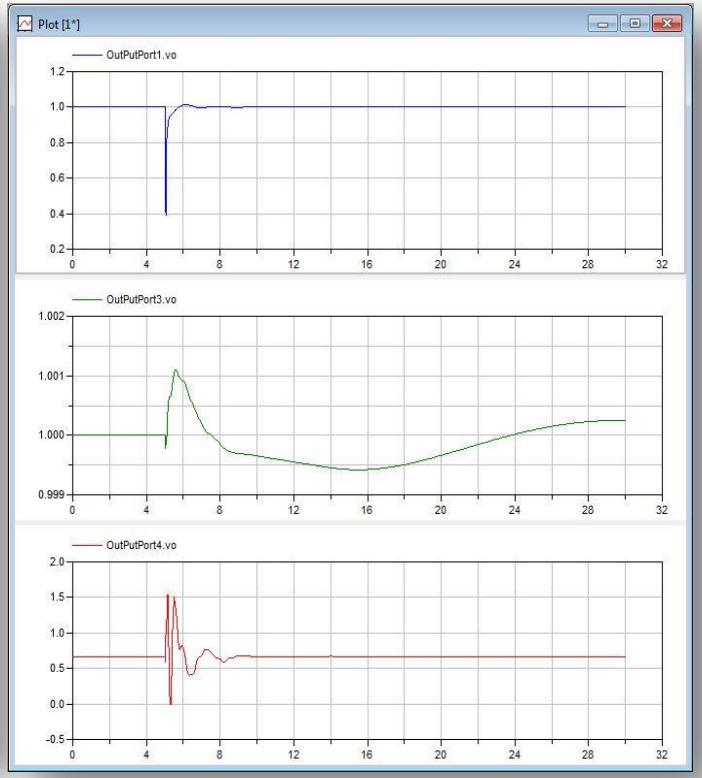

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Recommendations – Looking into the Future: Avoid Modeling Ambiguity

- **Possible solutions to ambiguity (cont'd)**
- FMI
  - Automotive industry has used the Flexible Mock-up Interface approach. Models are exported in a FMU (Functional Mock-up Unit).
  - FMUs can be imported in another environment and executed.
  - FMUs from different sources can cooperate at runtime in a co-simulation environment. FMI defines the interfaces for this to happen.
  - Caveat: co-simulation environment is needed. Would be difficult to do real-time simulation (in the case of Opal-RT Models).

  - OPAL-RT already support co-simulation for loosely coupled systems.
  - But
    - Co-Simulation is very difficult for tightly coupled system such as AC/DC circuit due to delays since simultaneous solution is required. OPAL-RT has developed SSN for this purpose.
    - The use of FMI for electrical network simulation still need to me demonstrated and it may happen that FMI is a good approach for loosely coupled simulation only (control systems and plant models with very different time constants).

Recommendations – Looking into the Future: Avoid Modeling Ambiguity

- **Possible solutions to ambiguity (Cont'd)**
- CIM-for-EMT
  - Would be similar to the Modelica approach, but it would be more difficult to share exact equations (or package them so that they are "closed").
  - As of now, CIM only defines the topology and system parameters, not the model equations

SmarTS Lab

Smart Transmission Systems Laboratory

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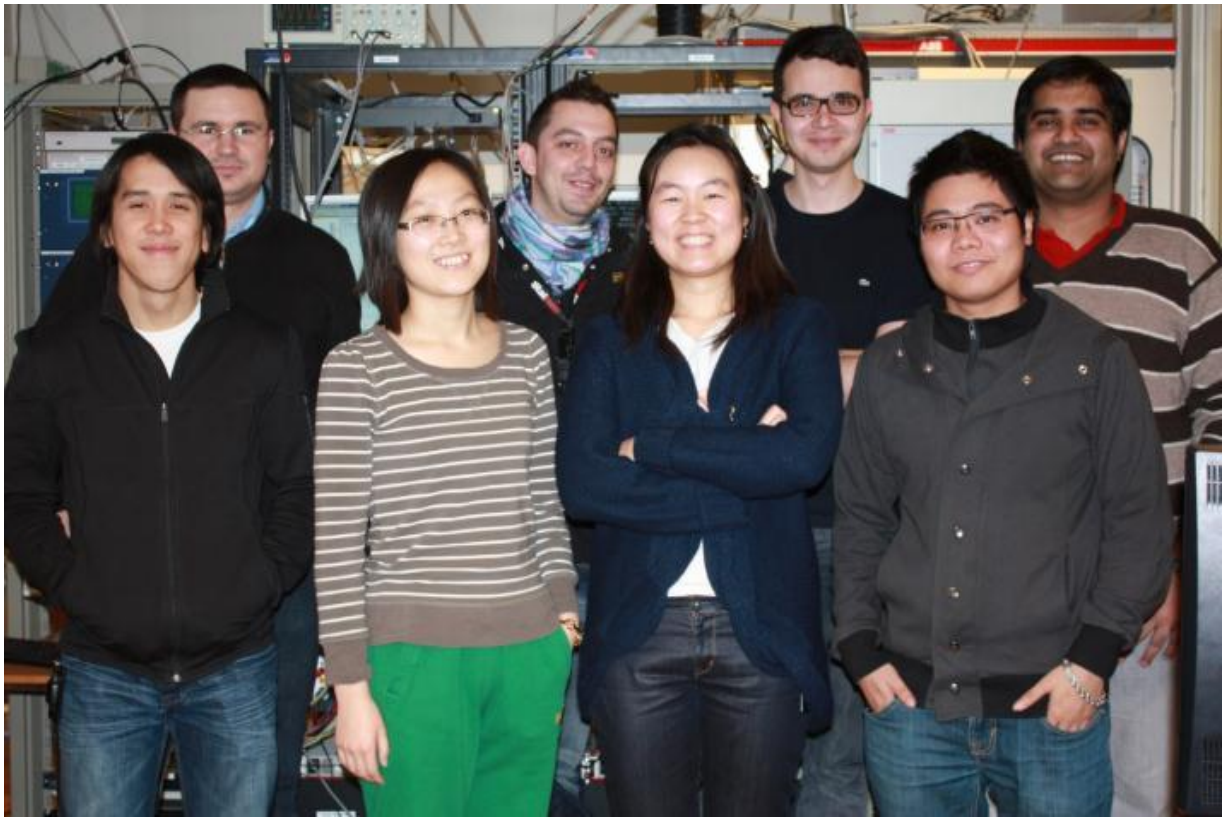

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Thank you!